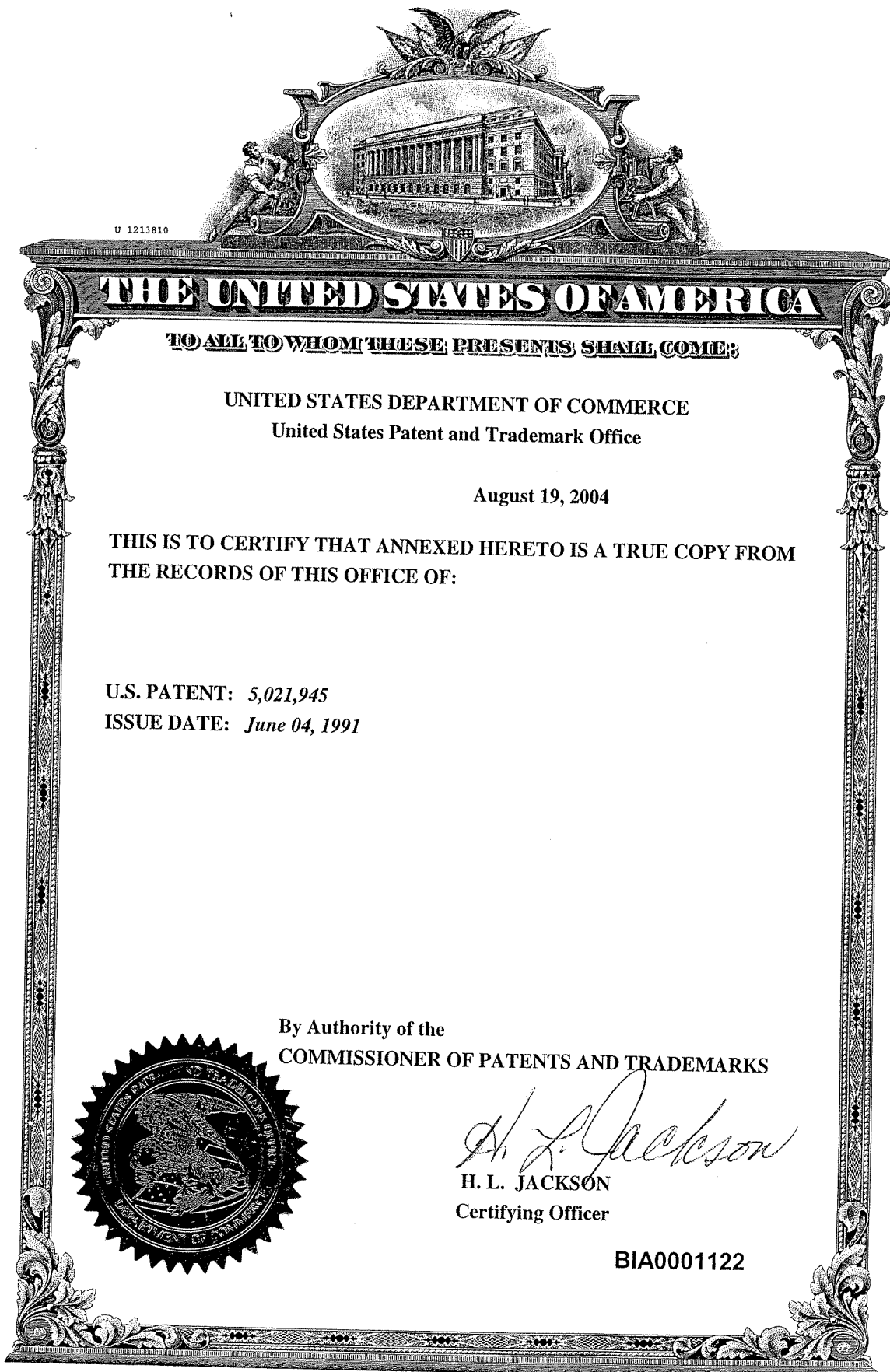


*BIAX Corporation v. Intel*  
**Civil Action No. 2:05-cv-184-TJW**

**EXHIBIT 2**  
**(PART 1)**  
**FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT**



**United States Patent** [19]**Morrison et al.**[11] **Patent Number:** **5,021,945**[45] **Date of Patent:** **Jun. 4, 1991**[54] **PARALLEL PROCESSOR SYSTEM FOR PROCESSING NATURAL CONCURRENCIES AND METHOD THEREFOR**[75] **Inventors:** Gordon E. Morrison, Denver; Christopher B. Brooks; Frederick G. Gluck, both of Boulder, all of Colo.[73] **Assignee:** MCC Development, Ltd., Boulder, Colo.[21] **Appl. No.:** 372,247[22] **Filed:** Jun. 26, 1989**Related U.S. Application Data**

[62] Division of Ser. No. 794,221, Oct. 31, 1985, Pat. No. 4,847,755.

[51] **Int. Cl.:** ..... G06F 15/16; G06F 9/38[52] **U.S. Cl.:** ..... 364/200; 364/230.3; 364/228.2; 364/262.4; 364/271.3[58] **Field of Search** ... 364/200 MS File, 900 MS File[56] **References Cited****U.S. PATENT DOCUMENTS**

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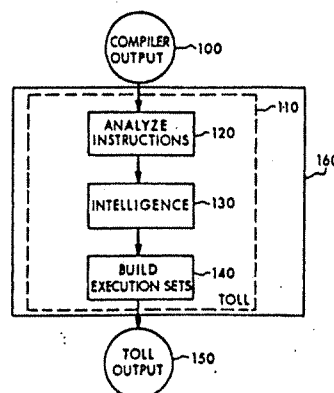
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**Primary Examiner**—Eddie P. Chan**Attorney, Agent, or Firm**—Hale and Dorr

[57]

**ABSTRACT**

A computer processing system containing a plurality of identical processor elements each of which does not retain execution state information from prior operations. The plurality of identical processor elements operate on a statically compiled program which, based upon detected natural concurrences in the basic blocks of the programs, provide logical processor numbers and an instruction firing time to each instruction in each basic block. Each processor element is capable of executing instructions on a per instruction basis such that dependent instructions can execute on the same or different processor elements. A given processor element is capable of executing an instruction from one context followed by an instruction from another context through use of shared storage resources.

**37 Claims, 17 Drawing Sheets****BIA0001123**

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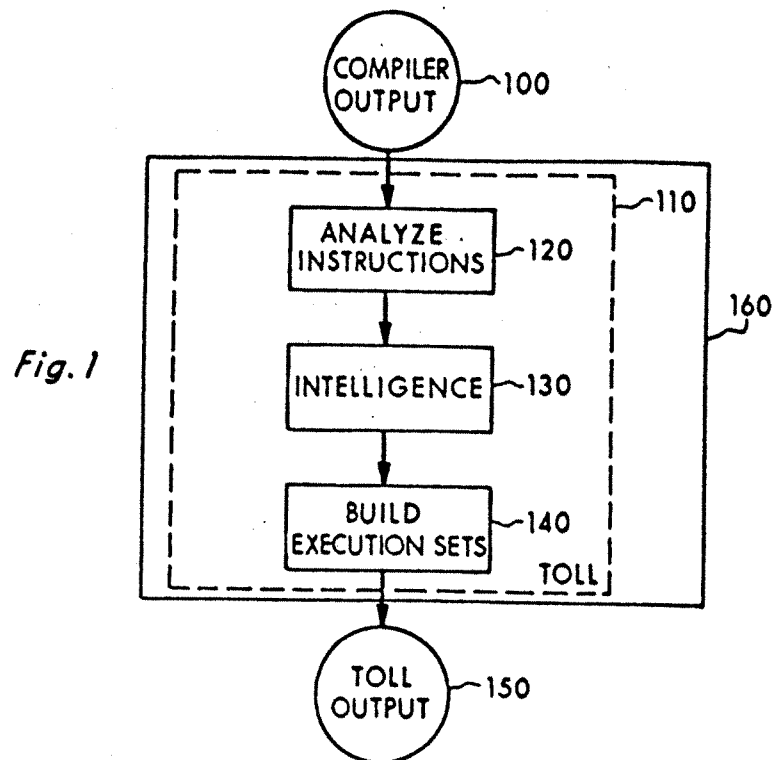
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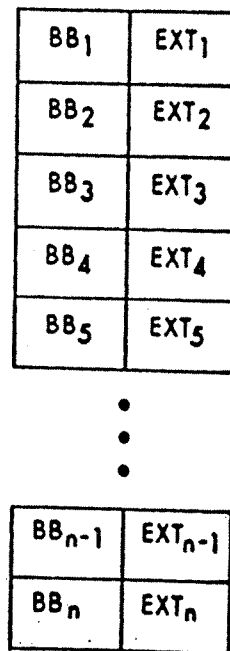
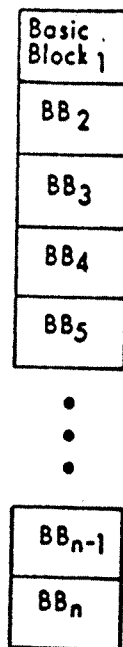
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*Fig. 2*  
*Prior Art*



*Fig. 3*

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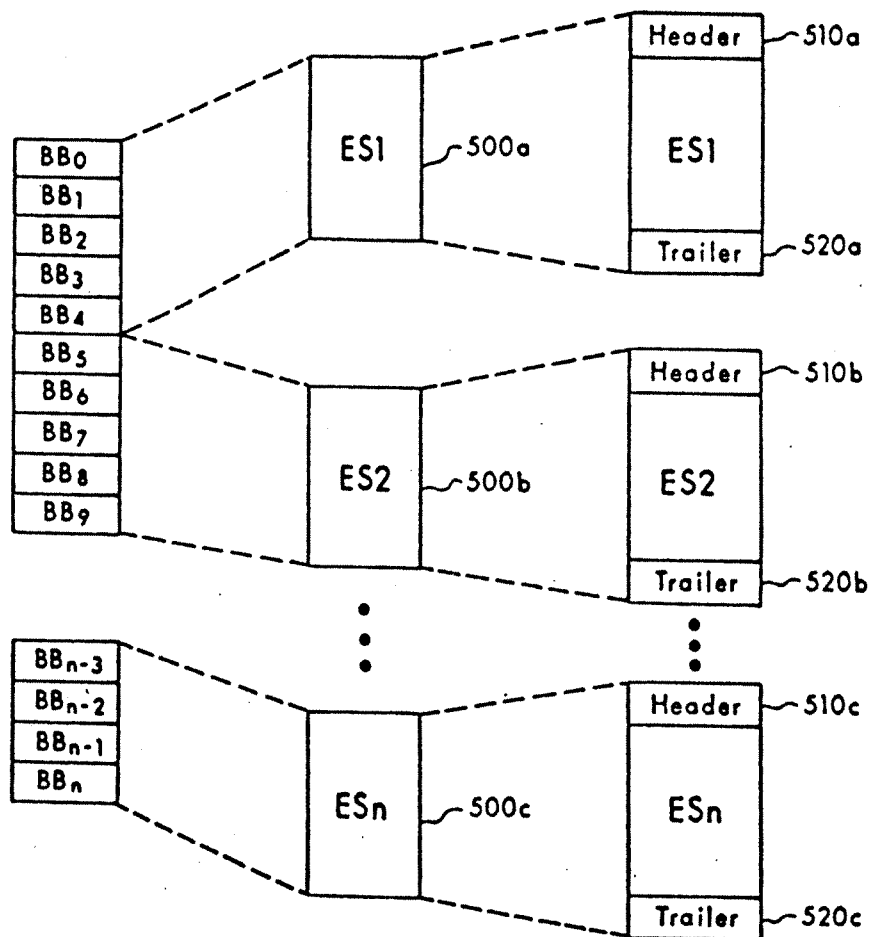
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Fig. 4

IO	LPN <sub>0</sub>	IFT <sub>0</sub>	SCSM <sub>0</sub>
I1	LPN <sub>1</sub>	IFT <sub>1</sub>	SCSM <sub>1</sub>
⋮			
I <sub>n</sub>	LPN <sub>n</sub>	IFT <sub>n</sub>	SCSM <sub>n</sub>

Fig. 5



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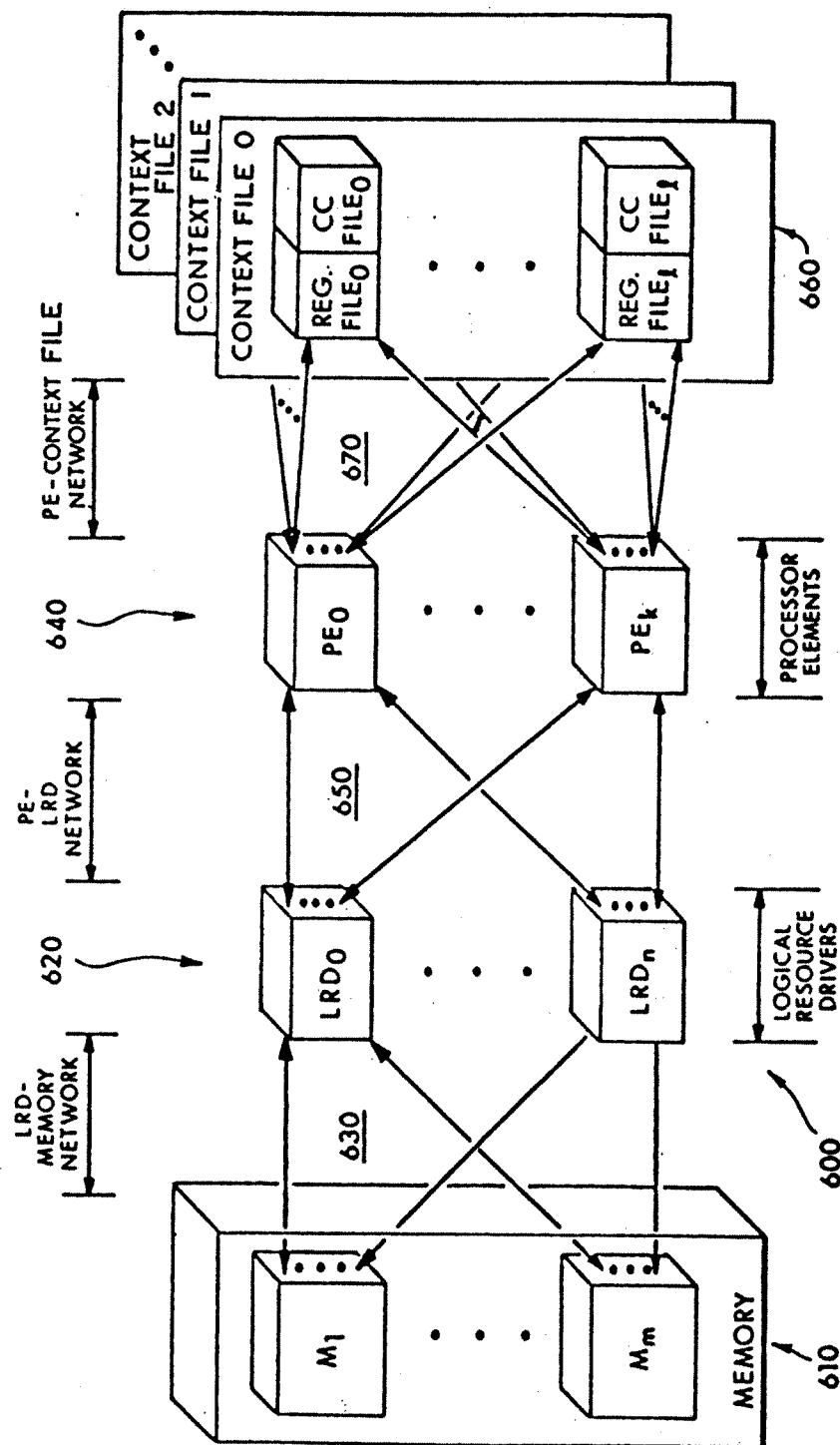
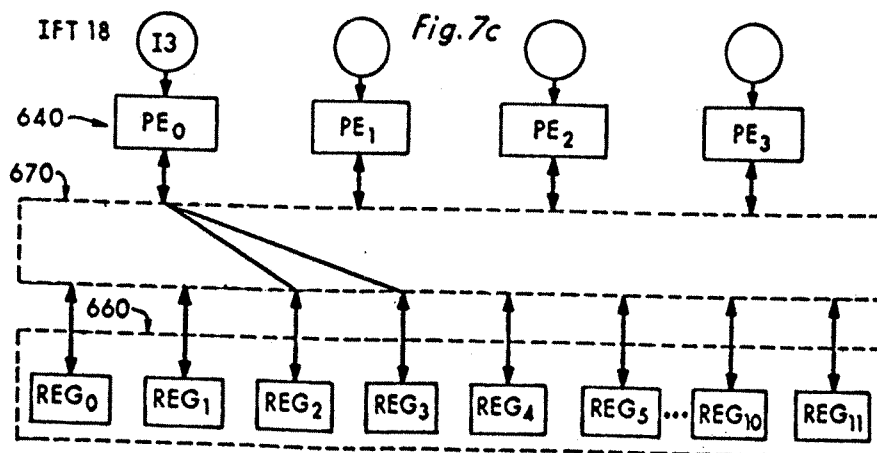
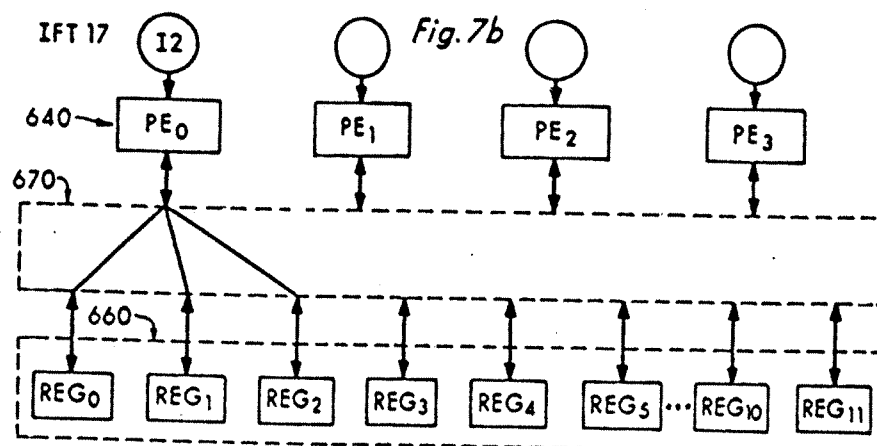
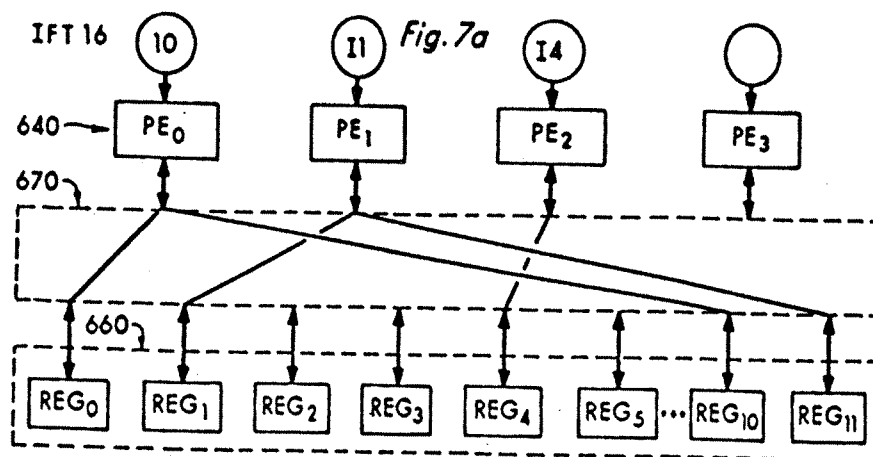


Fig. 6

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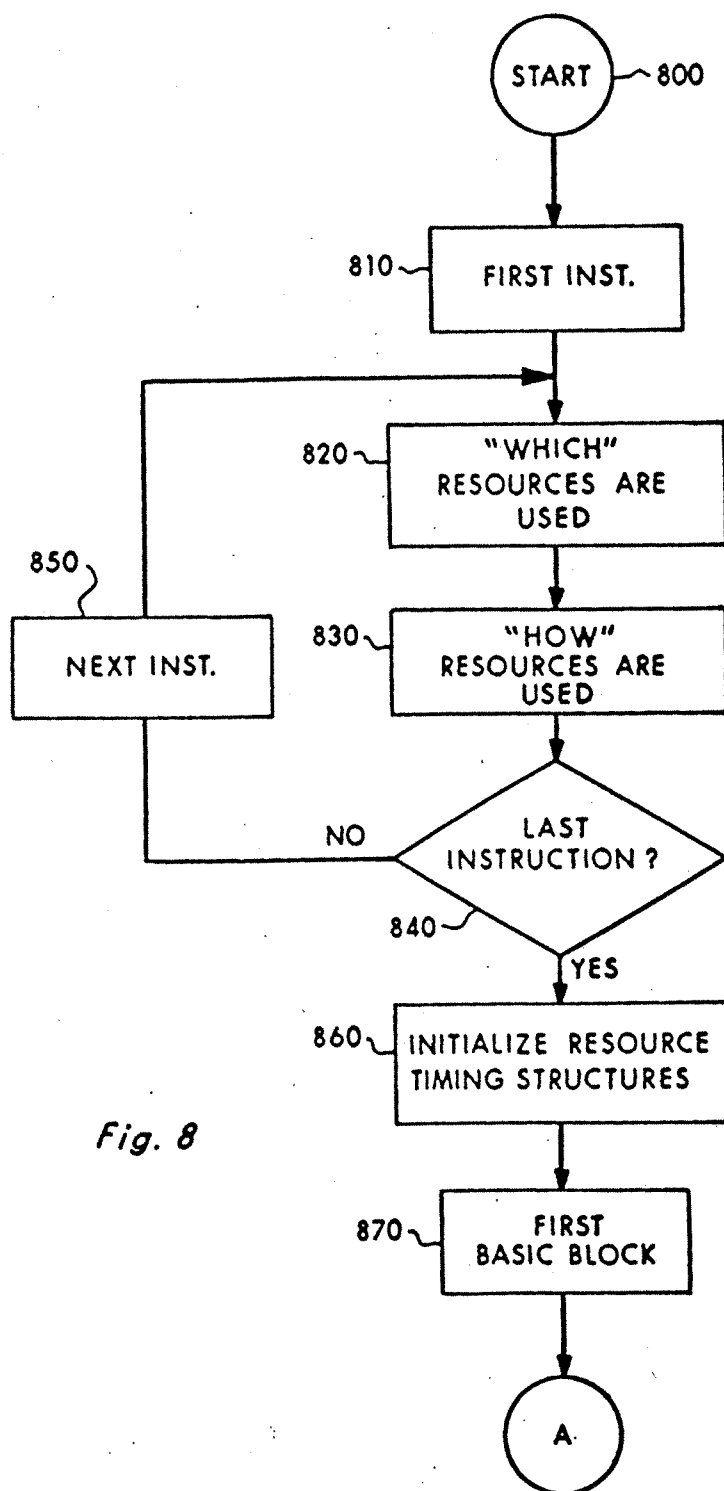


Fig. 8

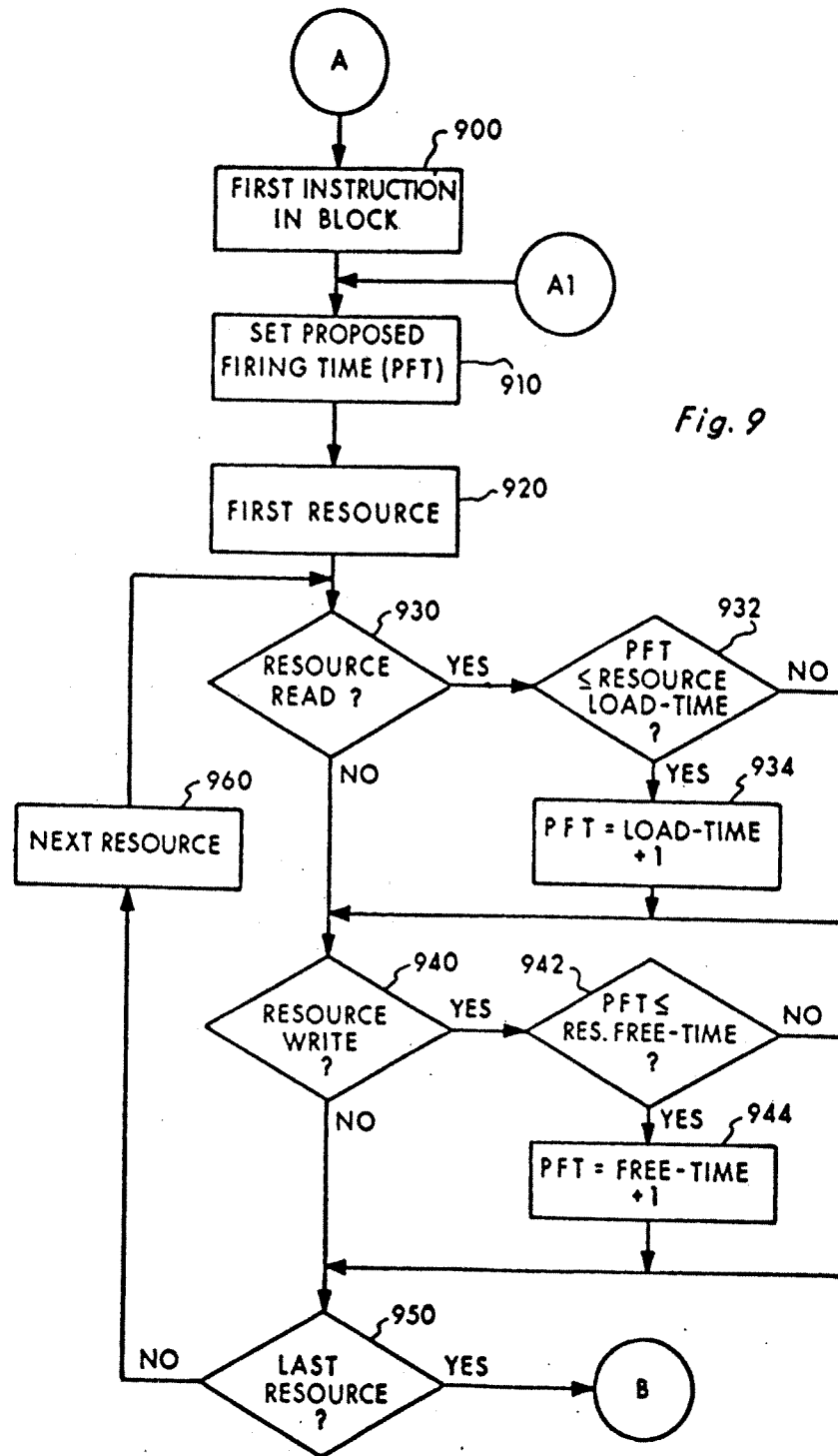
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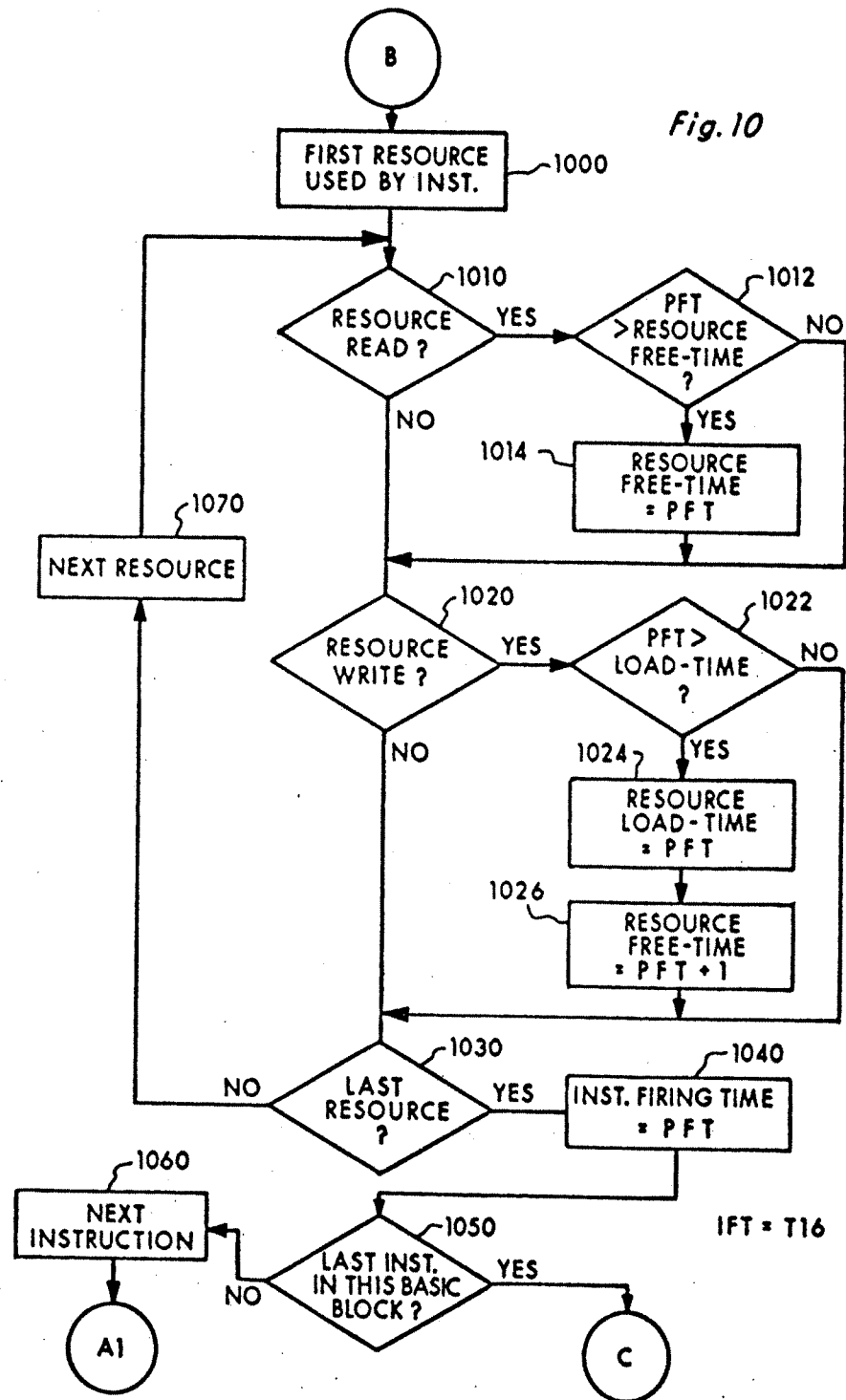
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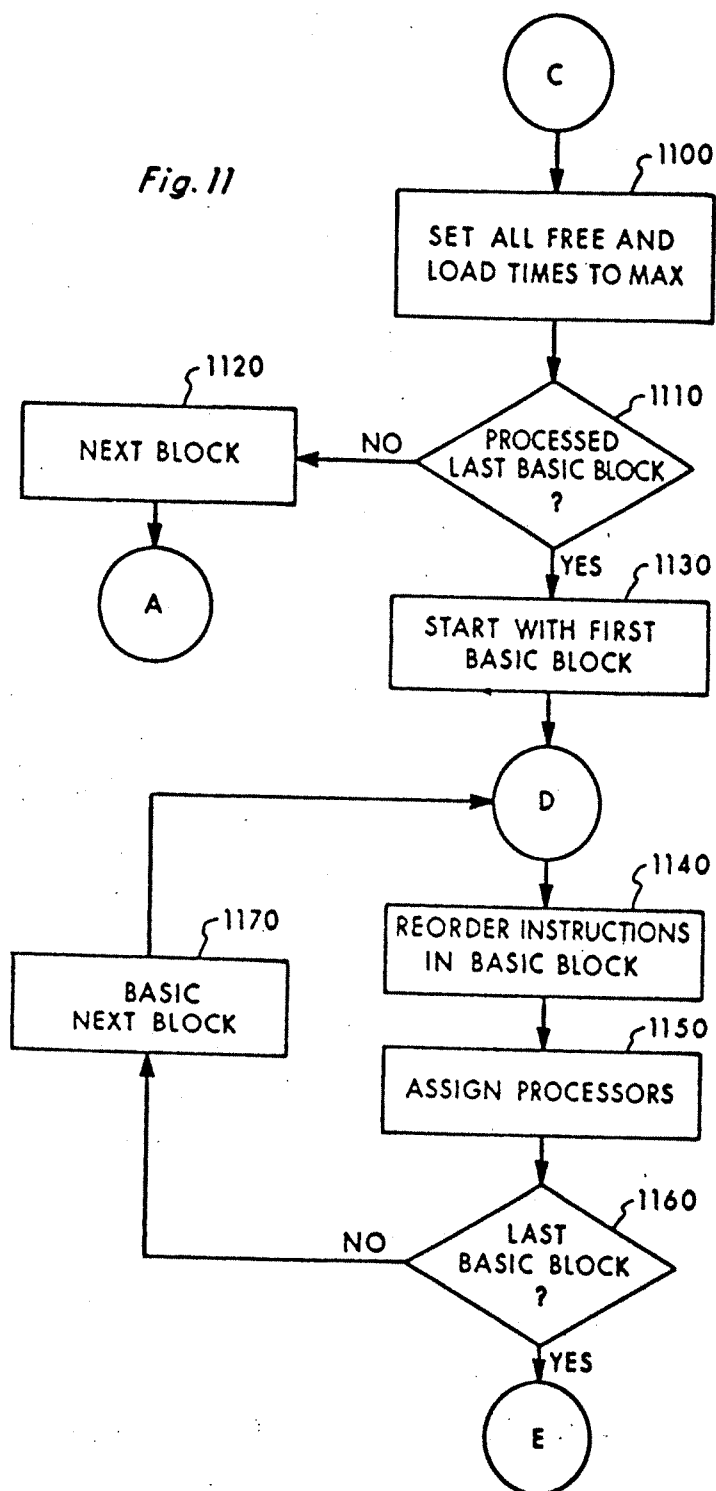
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Fig. 11



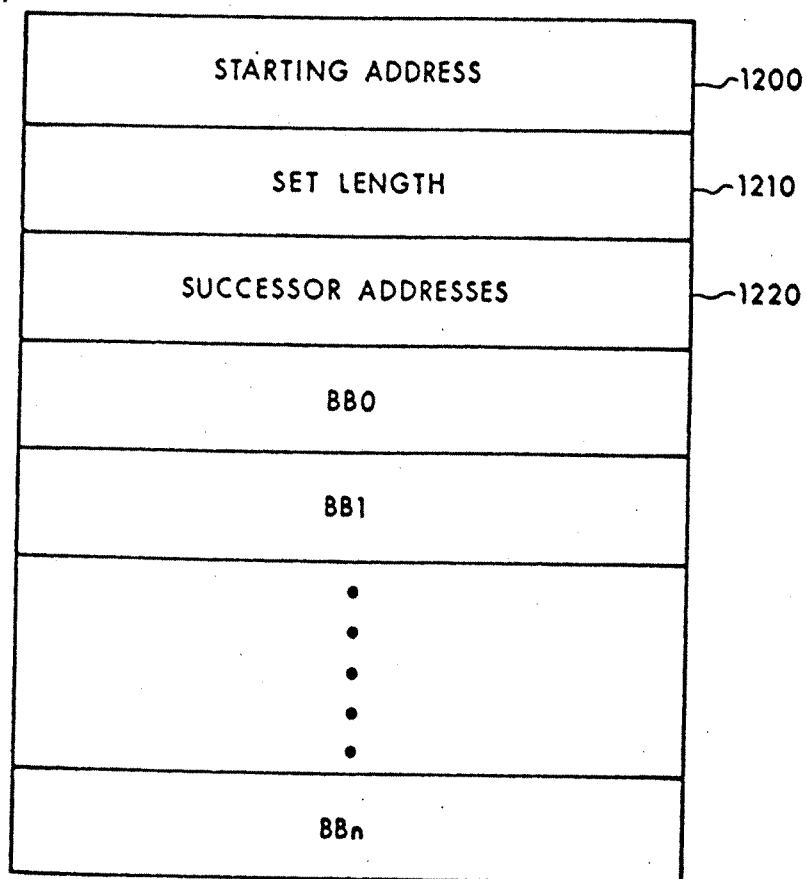
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*Fig. 12*

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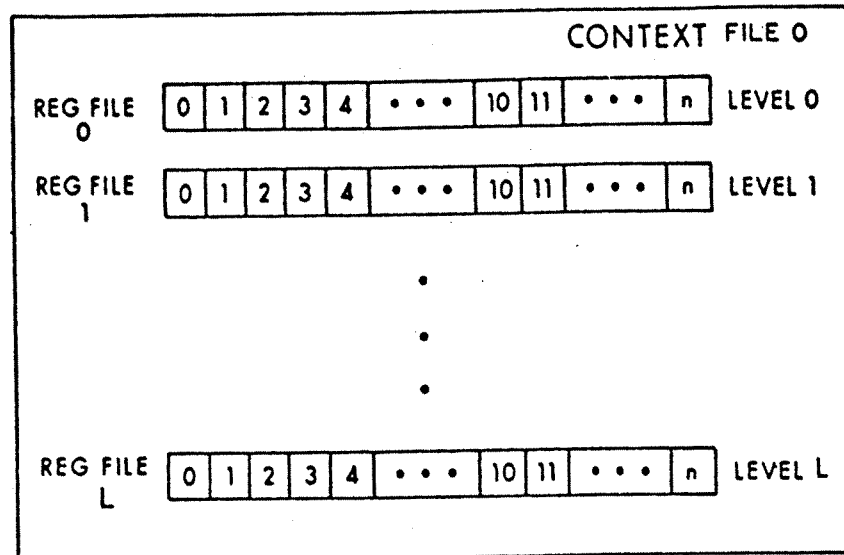


Fig. 13

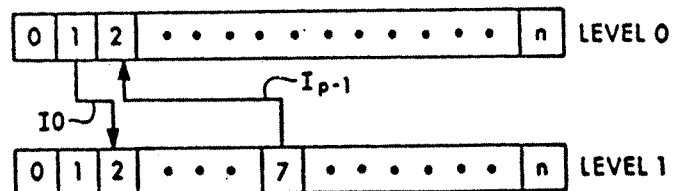


Fig. 14

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